CNT as FET

Nanotubes Types

- Single-walled
  - Armchair
  - Zigzag
- Double-walled
- Multi-walled

Nanotubes advantages over CMOS

- High carrier mobility.
- Suppress Short Channel Effect.

Carrier Mobility

- **CMOS**
  - The performance of CMOS depends on the mobility of both electrons and holes.
  - The effective mass of hole is heavier than that of electron so the mobility of holes is less than that of electron and this limits the performance of CMOS.
- **CNT**
  - Combining NMOS and PMOS results in high mobility for both electron and holes.
  - The fabrication process is complicated.

Short Channel Effect "SCE"

- **CMOS**
  - Doping concentration is increased to reduce SCE.
  - Increasing doping concentration will decrease electron mobility.
- **CNT**
  - SCE is suppressed due to the 1-D thin structure of CNT.

CNT-FET advantages

- Better control over channel formation.
- Better threshold voltage.
- Better sub-threshold slope.
- High electron mobility.
- High current density.
- High transconductance.

CNT-FET disadvantages

- Lifetime (degradation).
- Reliability.
- Production cost.

Operation

Gate Bias

- Conduct electrons for a positive bias
- Conduct holes for a negative bias.

Drain Current

- Increases with increasing applied gate bias.
- Increases with increasing drain bias unless the applied gate bias is below the threshold voltage.

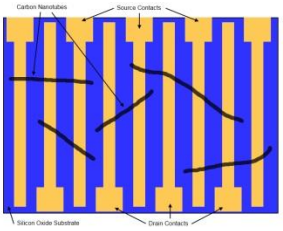
Fabrication

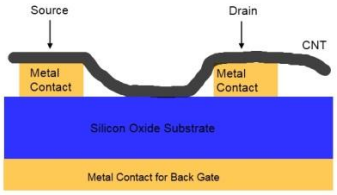
A. Back-gated

1. Put parallel strips of metal across a silicon dioxide substrate.
2. Depositing the CNTs on top of the metal strips in a random pattern.
3. A CNT that falls across two metal strips forms a basic FET.
4. One Metal strip is the source contact while the other is the drain contact.
5. Silicon oxide substrate is used as gate dielectric.
6. A metal contact is added on the back of the substrate to act as the gate contact.

Disadvantages of Back-gated

- The metal contact has very small contact to the CNT, since the nanotube just lay on top of it and the contact area was therefore very small.
- Due to the semiconducting nature of the CNT, a Schottkey Barrier forms at the metal-semiconductor interface, increasing the contact resistance.
- Gate dielectric thickness made it difficult to switch the transistor on and off using low voltages.





B. Top-gated

1. Single-walled carbon nanotubes deposited onto a silicon oxide substrate.
2. Individual nanotubes are located via scanning electron microscope.
3. Source and drain are patterned using high resolution electron beam lithography.
4. Deposition of top-gate dielectric.
5. The top gate contact is deposited on the gate dielectric.

Advantages of Top-gated

- Arrays of top-gated CNTFETs can be fabricated on the same wafer, since the gate contacts are electrically isolated from each other, unlike in the back-gated case.
- Due to the thinness of the gate dielectric, switching is easily done by lower gate voltage.

Disadvantages of Top-gated

- More complex fabrication process.